SMiTe: Precise QoS Prediction on Real-System SMT Processors to Improve Utilization in Warehouse Scale Computers

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Data centers are expensive

30%

Low utilization leads to inefficiency

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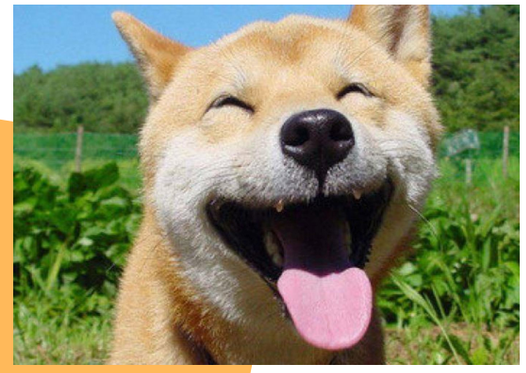

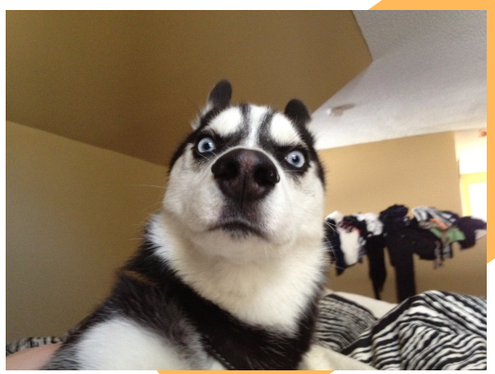

Private Cache

Functional Units

Memory Ports

Branch Predictor

TLB

Memory Bandwidth

Shared Cache

Utilization

No co-location

CMP co-location

SMT co-location

Resource Sharing

< 2%
Prediction Error

42%
Utilization Improvement

Session 5A
Wednesday at 9:50 A.M.